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EXAMINER	
TRUONG, LOAN	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,481	SMITH ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7, 9-10, 12-16, 24, 26-36, 38-63 and 65-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,10,12-16,24,26-36,38-63 and 65-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's argument filled on May 10, 2007 in application #10/804,481.

2. Claims 1-7, 9-10, 12-16, 24, 26-36, 38-63 and 65-85 are presented for examination. Claims 1, 24, 36, 55 are amended. Claims 11, 17-23, 25-27, 37 and 64 are cancelled. Claim 8 is not address in application. Claims 72-85 are newly added.

Response to Arguments

3. Applicant's arguments with respect to claims 1-7, 9-10, 12-16, 24, 26-36, 38-63 and 65-85 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 4-7, 9-10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Noy (US 7,114,111).

In regard to claim 1, Jibbe teaches an analyzer for capturing activity on a transmission medium, comprising:

(a) a data input port for receiving the activity from the transmission medium (*point to point connection exist between a single host computer and a single disk array controller, fig. 1, 105, 115, col. 5 lines 5-12)*

(b) replay logic for receiving the activity from the data input port and receiving stored activity from a trace buffer and sending out one or the other of these activities to the trigger logic, but not both (*if state variable P/A is set to one the process next reads the template data structure generated and performs a performance analysis and if P/A is set to zero the process is next operative to play the template data structure file back on the reference system, fig. 3, 330, 325, col. 9 lines 31-46),*

(c) a trace buffer for receiving activity from said replay logic and storing it (*set of template data structures is stored in a data file, col. 1-5)*, and for sending stored activity to said replay logic (*template data structure may be played out to emulate the behavior of a host computer, col. 9 lines 46-49)* and to a data output port (*generates an output which includes a set of template data structure, fig. 3, 315, col. 9 lines 2-4),*

(d) trigger logic for comparing the pattern of activity from the replay logic with a user-defined pattern of activity and indicating when they match (*search through a captured data file for a specific event or to specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4)*,

(e) trace buffer control logic for causing activity from said replay logic to be either read from or written to said trace buffer (*record button is to capture data as observed by host-side monitor and the play button is used to caused on a sequence of data packets capture to be reproduced in the reference system, col. 8 lines 5-35)*,

(f) a data output port for transferring stored activity in the trace buffer elsewhere for processing or display (*output is preferably stored in a data file but stream I/O may be used, col. 9 lines 4-5)*, and

(g) a control port for controlling modes of operation of the analyzer and for accepting user-defined patterns for triggering (*monitor and analyzes data transfer generated in the references system may be practiced with affair amount of intervention from the technician using GUI window and the submenus, fig. 2, 200, col. 9 lines 53-64).*

Jibbe does not explicitly teach the analyzer for capturing activity on a transmission medium wherein activity events are stored at a fixed frequency, thereby providing a fixed time between events.

Noy teaches the method of maximizing test coverage by implementing the collection of data related to temporal coverage such as triggering event is optionally a fixed, predefined sampling time (*col. 8 lines 38-52).*

It would have been obvious to modify the method Jibbe by adding Noy method of maximizing test coverage. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would allow temporal coverage (*col. 8 lines 40-46).*

In regard to claim 4, Jibbe teaches an analyzer as recited in claim 1 further comprising selective capture logic for causing the trace buffer control logic to cause the activity from the replay logic to be written to the trace buffer only when the activity from said replay logic matches a second user-defined pattern of activity (*user selects record button to initiate data capture, col. 8 lines 45-65).*

In regard to claim 5, Jibbe teaches an analyzer as recited in claim 4 wherein said selective capture logic is capable of causing information about the type of activity from the replay logic that caused the activity to be written to said trace buffer to be incorporated into the activity stored in the trace buffer (*template data structure include a fourth field to stores input and output negotiation information respectively in a subfield, fig. 5, 520-522, col. 14 lines 12-24).*

In regard to claim 6, Jibbe teaches an analyzer as recited in claim 4 further comprising a timestamp counter for creating information about the time of occurrence of each activity event from the replay logic, so that such information may be incorporated into the activity stored in said trace buffer (*eight field of the template data structure stores the statistical information such*

as time-stamp associated with a data transfer, fig. 5, 540, col. 14 lines 31-33).

In regard to claim 7, Jibbe teaches an analyzer as recited in claim 6, wherein said trigger logic includes time counters for incorporating the relative time of occurrence of an activity event as part of its activity pattern comparison, and wherein said replay logic uses said stored time-of-occurrence information to control the timing of the replay (*a time button is used to enter or read a time representative of the beginning of a file or a specific event within a file in the system analyzer, fig. 2, 210, col. 7 lines 21-41).*

In regard to claim 9, Jibbe teaches an analyzer as recited in claim 6 wherein said replay logic uses the stored time-of-occurrence information to control the timing of the replay (*a time button is used to enter or read a time representative of the beginning of a file or a specific event within a file in the system analyzer, fig. 2, 210, col. 7 lines 21-41).*

In regard to claim 10, Jibbe teaches an analyzer as recited in claim 9 further comprising a replay output port for sending the activity from the replay logic to a transmission medium (*a view button caused certain types of information relating to data transfer activity to be displayed, fig. 2, 225, col. 7 lines 45-53).*

In regard to claim 12, Jibbe teaches an analyzer as recited in claim 1 wherein said trigger logic is able to recognize, for comparison purposes, patterns of activity that consist of a single event and patterns of activity that consist of a sequence of events (*search through a captured*

data file for a specific event or to specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4).

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5. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Noy (US 7,114,111) in further view of Nelson et al. (US 6,928,108).

In regard to claim 2, Jibbe and Noy does not explicitly teach an analyzer as recited in claim 1, wherein said trace buffer control logic includes logic for overwriting previously stored activity with new activity.

Nelson et al. teach the modem with firmware upgrade feature implementing a protect switch when not enable would not prevent overwriting of the program area of the flash prom (*col. 13 lines 1-7).*

It would have been obvious to modify the analyzer of Jibbe and Noy by adding Nelson et al. protect switch. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would provide a back door to allow access to the area of the flash PROM where the boot control program is stored (*col. 13 lines 1-7).*

In regard to claim 3, Jibbe and Noy does not explicitly teach an analyzer as recited in claim 1 wherein said trace buffer control logic includes logic for avoiding overwriting previously stored activity with new activity.

Nelson et al. teach the modem with firmware upgrade feature implementing a protect switch when enable would not prevent erroneous overwriting of the boot control program area (*col. 13 lines 1-7).*

It would have been obvious to modify the analyzer of Jibbe and Noy by adding Nelson et al. protect switch. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would prevent erroneous overwriting (*col. 13 lines 1-7).*

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6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Noy (US 7,114,111) in further view of Bucher et al. (US 2001/0016925).

In regard to claim 13, Jibbe and Noy does not explicitly teach an analyzer as recited in claim 1 wherein said trigger logic includes at least one counter for counting the number of occurrences of an activity event as part of its activity pattern comparison.

Bucher et al. teach a deep trace memory system for a protocol analyzer implementing a read and a write counter (*paragraph 0030, fig. 4).*

It would have been obvious to modify the replay analyzer of Jibbe and Noy by adding Butcher et al. deep trace memory system for a protocol analyzer. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would allow dual port memory to act as a fifo *(paragraph 0030).*

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7. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Noy (US 7,114,111) in further view of Blatter et al. (US 6,236,694).

In regard to claim 14, Jibbe and Noy does not explicitly teach an analyzer as recited in claim 1 wherein said trigger logic includes time counters for using the relative time of occurrence of an activity event as part of its activity pattern comparison.

Blatter et al. teach the bus and interface system implementing a compares of the replayed timestamp value with a continuously changing count value produced by counting a free running oscillator *(col. 9 lines 13-24).*

It would have been obvious to modify the analyzer of Jibbe and Noy by adding Blatter et al. bus and interface system. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would facilitate the elimination of data timing perturbations and discontinuities resulting

from record/replay processing and enable the recorded signal timing to be restored (*col. 1 lines 63-67).*

In regard to claim 15, Jibbe and Noy does not explicitly teach an analyzer as recited in claim 14 wherein said replay logic uses the fixed time between events to send the stored activity out with the same timing with which it was received at the data input port.

Blatter et al. teach the bus and interface system implementing a compares of the replayed timestamp value with a continuously changing count value produced by counting a free running oscillator (*col. 9 lines 13-24)* with suitable timing reference and relatively precise timing reference for use during reproduction (*col. 1 lines 59-63).*

Refer to claim 14 for motivational statement.

In regard to claim 16, Jibbe and Noy does not explicitly teach an analyzer as recited in claim 15 further comprising a replay output port for sending the activity from the replay logic to a transmission medium.

Blatter et al. teach the bus and interface system implementing a compares of the replayed timestamp value with a continuously changing count value produced by counting a free running oscillator (*col. 9 lines 13-24)* with suitable timing reference and relatively precise timing reference for use during reproduction (*col. 1 lines 59-63).*

Refer to claim 14 for motivational statement.

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8. Claims 24, 27-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Lee et al. (US 6,377,643).

In regard to claim 24, Jibbe teaches an analyzer for analyzing activity on a transmission medium, comprising:

(a) a data input port for receiving the activity from the transmission medium (*point to point connection exist between a single host computer and a single disk array controller, fig. 1, 105, 115, col. 5 lines 5-12)* ,

(b) a trace buffer for storing said received activity (*set of template data structures is stored in a data file, col. 1-5)*,

(c) replay logic for replaying stored activity in said trace buffer (*if state variable P/A is set to zero the process is next operative to play the template data structure file back on the reference system, fig. 3, 330, 325, col. 9 lines 31-46)*,

(d) a control port for permitting a user to define a data pattern to be matched in said received activity (*monitor and analyzes data transfer generated in the references system may be practiced with affair amount of intervention from the technician using GUI window and the submenus, fig. 2, 200, col. 9 lines 53-64)*, and

(e) trigger logic for triggering an action based on a match between said data pattern and said replayed activity (*specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4)* wherein said trigger logic includes the ability to latch address information of said match to a storage area (*fifth field stores address information, fig. 5, 528, col. 14 lines 24-26).*

Jibbe does not teach an analyzer comprising trigger logic has the ability to find multiple matches in said replayed activity.

Lee et al. teach the method of comparing a pattern matching sync signal output from a sync pattern detector according to clocks of the parallel clock generator (*col. 3 lines 6-10).*

It would have been obvious to modify the method Jibbe by adding Lee et al. pattern matching. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would solve the problem of deviation of a window caused by erroneous detection of a sync signal and disagreement of the numbers of clocks by using a specified window (*col. 1 lines 56-60).*

In regard to claim 27, Jibbe teaches an analyzer as recited in claim 24 further comprising means for performing additional analysis of said stored activity (*filters useless information from the captured data, fig. 3, 310, col. 8 lines 65-67).*

In regard to claim 28, Jibbe teaches an analyzer as recited in claim 27 wherein said means for performing additional analysis includes the ability to create a histogram (*statistical information relating to performance is tabulated and presented to the user, col. 9 lines 39-41).*

In regard to claim 29, Jibbe teaches an analyzer as recited in claim 27 wherein said means for performing additional analysis uses the same circuitry as said replay and trigger logic (*host-*

side monitor, fig. 1, 125).

In regard to claim 30, Jibbe teaches an analyzer as recited in claim 27 wherein said means for performing additional analysis includes real time protocol monitoring (*analyzing information related to time stamps, col. 9 lines 34-38).*

In regard to claim 31, Jibbe teaches an analyzer as recited in claim 27 wherein said means for performing additional analysis includes real time statistical analysis (*statistical data may be used to tune simulation or system parameters, col. 9 lines 38-43).*

In regard to claim 32, Jibbe teaches an analyzer as recited in claim 27 wherein said means for performing additional analysis includes traffic generation (*analyzing information related to data transfer rate, col. 9 lines 34-38).*

In regard to claim 33, Jibbe teaches an analyzer as recited in claim 24 wherein said replay logic function is carried out by a computer chip (*reproduced and analyzed in the reference system, col. 7 lines 7-9)* other than a microprocessor (*source computer, col. 7 lines 7-9).*

In regard to claim 34, Jibbe teaches an analyzer as recited in claim 24 wherein said replay logic is implemented in computer hardware (*host-side monitor or backside monitor, fig. 1, 125, 140).*

In regard to claim 35, Jibbe teaches an analyzer as recited in claim 24 wherein the analyzer used shared hardware to perform real time monitoring, preparation of statistical information, post-capture analysis and replaying saved traffic from a transmission medium (*some cases it may be desirable to select both record button and play button simultaneously to allow captured data file to be played and a new file to be captured and allows recreated event to be analyzed in non-real-time, col. 8 lines 36-44).*

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9. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Lee et al. (US 6,377,643) in further view of Bucher et al. (US 6,393,587).

In regard to claim 26, Jibbe and Lee et al. does not teach an analyzer as recited in claim 24 wherein said replay function terminates on finding a match.

Bucher et al. teach the protocol analyzer implementing a search engine operating until a match is found the terminating the search (*fig. 6, 60, col. 8 lines 20-22).*

It would have been obvious to modify the analyzer of Jibbe and Lee et al. by adding Bucher et al. protocol analyzer. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would allow hardware search engin to search the entire contents of the trace bufer for a pecified data pattern in less than 10 seconds (*col. 4 lines 44-48).*

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10. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Bucher et al. (US 2001/0016925) in further view of Blatter et al. (US 6,236,694) in further view of Dwyer (US 6,820,251).

In regard to claim 44, Jibbe teaches an analyzer as recited in claim 43 wherein said terms are selected from the group consisting addresses and data transfers (*subfields holds the information extracted by data parser, fig. 5, col. 14 lines 12-34).*

Jibbe, Bucher et al. and Blatter et al. does not teach the term being a command packets and signal assertions.

Dwyer teaches the system for software recovery by implementing a check for an assertion and function call (*fig. 7, 144, 146, col. 7 lines 1-13).*

It would have been obvious to modify the analyzer of Jibbe, Bucher et al. and Blatter et al. by adding Dwyer system for software recovery. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would check for validity (*col. 6 lines 36-37).*

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11. Claims 36, 38-43, 45, 48-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Bucher et al. (US 2001/0016925) in further view of Blatter et al. (US 6,236,694).

In regard to claim 36, Jibbe teaches a replay analyzer comprising:

a data input port for receiving data (*point to point connection exist between a single host computer and a single disk array controller, fig. 1, 105, 115, col. 5 lines 5-12)*, a trace buffer for storing data (*set of template data structures is stored in a data file, col. 1-5)*, term logic (*specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4)*,

selective capture logic for determining which data to store in said trace buffer (*filter information from captured data, fig. 3, 310, col. 8 lines 66-67)*,

replay logic for replaying data stored in said trace buffer (*if state variable P/A is set to zero the process is next operative to play the template data structure file back on the reference system, fig. 3, 330, 325, col. 9 lines 31-46)*, and

a trigger for triggering on a match with replayed data (*specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4)*.

Jibbe does not explicitly teach the replay analyzer comprising at least one event statistic counter.

Bucher et al. teach a deep trace memory system for a protocol analyzer implementing a read and a write counter (*paragraph 0030, fig. 1, 20, 22).*

It would have been obvious to modify the replay analyzer of Jibbe by adding Butcher et al. deep trace memory system for a protocol analyzer. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would allow dual port memory to act as a fifo (*paragraph 0030).*

Jibbe and Bucher et al. does not explicitly teach a timestamp counter.

Blatter et al. teach the bus and interface system implementing a compares of the replayed timestamp value with a continuously changing count value produced by counting a free running oscillator (*col. 9 lines 13-24).*

It would have been obvious to modify the analyzer of Jibbe and Butcher et al. by adding Blatter et al. bus and interface system. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would facilitate the elimination of data timing perturbations and discontinuities resulting from record/replay processing and enable the recorded signal timing to be restored (*col. 1 lines 63-67).*

In regard to claim 38, Jibbe and Bucher et al. does not explicitly teach an analyzer as recited in claim 36 further comprising a timestamp upcounter.

Blatter et al. teach the bus and interface system implementing a compares of the replayed timestamp value with a continuously changing count value produced by counting a free running oscillator (*col. 9 lines 13-24).*

Refer to claim 36 for motivational statement.

In regard to claim 39, Jibbe teaches an analyzer as recited in claim 36 further comprising a control port for allowing user control of the analyzer (*GUI window, fig. 2, 200).*

In regard to claim 40, Jibbe teaches an analyzer as recited in claim 36 wherein said replay trigger includes the ability to identify specific data values or events (*data is played back*

preferably at time 00:00:00 or a specific event within a file, col. 7 lines 31-35).

In regard to claim 41, Jibbe teaches an analyzer as recited in claim 36 further comprising an adapter pod for connecting the analyzer to a transmission medium (*host-side hub connected to the host-side monitor, fig. 1, 110, 125).*

In regard to claim 42, Jibbe teaches an analyzer as recited in claim 36 wherein said term logic performs pattern recognition for the analyzer (*specify a trigger event, col. 8 lines 1-4).*

In regard to claim 43, Jibbe does not explicitly teach an analyzer as recited in claim 36 wherein said event statistic counter provides long term statistics regarding types of events that are occurring, each event type being defined by a term.

Bucher et al. teach a deep trace memory system for a protocol analyzer implementing a searching process with search direction set under logic step with 16 desired data words and 16 don't care words (*paragraph 0038).*

It would have been obvious to modify the replay analyzer of Jibbe by adding Butcher et al. deep trace memory system for a protocol analyzer. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would help to locate specified data patterns within the trace buffer without the need to download data to the main memory of the host processor (*paragraph 0014).*

In regard to claim 45, Jibbe teaches an analyzer as recited in claim 36 wherein said selective capture logic uses terms from said term logic to capture only incoming activity that matches predefined or user patterns (*specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4).*

In regard to claim 48, Jibbe teaches an analyzer as recited in claim 36 wherein the analyzer has a capture mode and a replay mode that are user-selectable (*GUI window with record and play button, fig. 2, 220, 235).*

In regard to claim 49, Jibbe teaches an analyzer as recited in claim 36 wherein said replay logic permits selection data flow source and direction (*when data is play back data is extracted from the path/file specified by this button in the GUI window, col. 7 lines 21-32).*

In regard to claim 50, Jibbe teaches an analyzer as recited in claim 49 wherein said data flow source and direction may be selected from (i) a flow starting at said data input port (*specific one of host, fig. 1, 105, col. 8 lines 15-35)*, and to said term logic (*specify a trigger event, col. 8 lines 1-4)* and said trace buffer (*set of template data structures is stored in a data file, col. 1-5)*, or (ii) from said trace buffer (*set of template data structures is stored in a data file, col. 1-5)* to said trigger (*specific event or trigger event, col. 8 lines 1-4).*

In regard to claim 51, Jibbe teaches an analyzer as recited in claim 36 further comprising a replay output port (*view button causes a display window to be display, col. 7 lines 45-49)*

In regard to claim 52, Jibbe teaches an analyzer as recited in claim 51 further comprising an output adapter pod (*Host-side hub, fig. 1, 110)*; wherein said replay output port (*host-side monitor, fig. 1, 125)* and said output adapter pod are in data communication with each other so that data may exit the analyzer through said output port and through said output adapter pod to a bus in order to facilitate traffic generation on a bus (*first traffic flow involves data transfers between host computer and devices such as disk array controller, col. 6 lines 9-16).*

In regard to claim 53, Jibbe teaches an analyzer as recited in claim 52 wherein activity stored in said trace buffer may be used to generate traffic on a bus (*play button is used to direct a sequence of data packets captured from source computer system to be reproduced in the reference system, col. 8 lines 16-19).*

In regard to claim 54, Jibbe teaches an analyzer as recited in claim 36 further comprising a control port through which a local (*support technicians evaluate their own system, col. 7 lines 56-60)* or remote user can configure analyzer logic (*technical support facility, col. 7 lines 6-20).*

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12. Claims 46-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Bucher et al. (US 2001/0016925) in further view of Blatter et al. (US 6,236,694) in further view of Rivoir (US 6,105,087).

In regard to claim 46, Jibbe, Bucher et al. and Blatter et al. does not teach an analyzer as recited in claim 36 further comprising a trigger sequencer that is capable of triggering said trigger.

Rivori teaches an event recognition by a state machine implementing a sequencer state machine to initiates a corresponding bus transaction when it reaches a certain predefined state (*col. 2 lines 47-53).*

It would have been obvious to modify the apparatus of Jibbe, Butcher et al. and Blatter et al. by adding Rivoir event recognition. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would provide an improved tool for monitoring and/or processing events occurring in a data processing unit (*col. 2 lines 19-21).*

In regard to claim 47, Jibbe, Bucher et al. and Blatter et al. does not teach an analyzer as recited in claim 46 wherein said trigger sequencer can terminate writing to or reading from said trace buffer.

Rivori teaches an event recognition by a state machine implementing a sequencer state machine to initiates a corresponding bus transaction when it reaches a certain

predefined state (*col. 2 lines 47-53)* wherein the event recognizer coupled via a line to a memory for controlling a read/write access of the memory (*col. 2 lines 9-12).*

Refer to claim 46 for motivational statement.

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13. Claims 55-63 and 65-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Rivoir (US 6,105,087).

In regard to claim 55, Jibbe teaches an analyzer comprising:

a control port to permit user configuration of the analyzer (*GUI window, fig. 2, 200)*,

a data input port for receiving data from a transmission medium (*point to point connection exist between a single host computer and a single disk array controller, fig. 1, 105, 115, col. 5 lines 5-12)*,

a trace buffer for storing data from said data input port (*set of template data structures is stored in a data file, col. 1-5)*,

trace buffer control logic for determining which data from said data input port to store in said trace buffer (*filter useless information from the captured data, fig. 3, 310, col. 8 lines 66-67)*,

replay logic for replaying data stored in said trace buffer (*if state variable P/A is set to zero the process is next operative to play the template data structure file back on the reference system, fig. 3, 330, 325, col. 9 lines 31-46)*, and

term logic for matching a desired term with replayed data (*specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4).*

Jibbe does not explicitly teach an analyzer comprising a trigger sequencer that uses state machine architecture to trigger on an event.

Rivori teaches an event recognition by a state machine implementing a sequencer state machine to initiates a corresponding bus transaction when it reaches a certain predefined state (*col. 2 lines 47-53).*

It would have been obvious to modify the apparatus of Jibbe by adding Rivoir event recognition. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would provide an improved tool for monitoring and/or processing events occurring in a data processing unit (*col. 2 lines 19-21).*

In regard to claim 56, Jibbe teaches an analyzer as recited in claim 55 further comprising a selective capture feature (*filtering from the captured data, fig. 3, 310, col. 8 lines 66-67).*

In regard to claim 57, Jibbe teaches an analyzer as recited in claim 55 wherein said term logic performs event pattern recognition (*specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4).*

In regard to claim 58, Jibbe teaches an analyzer as recited in claim 57 wherein said events are selected from the group consisting of high, low, rising edge, falling edge, either edge and

dontcare (*probe is connected to a test point to collect a bit of information each clock interval, col. 1 lines 38-41).*

It is inherent data capture or monitor for the event recognition at each clock interval, the selection of high, low, rising edge, falling edge, either edge and don't care is a design choice.

In regard to claim 59, Jibbe teaches an analyzer as recited in claim 55 further comprises selective capture logic (*filtering from the captured data, fig. 3, 310, col. 8 lines 66-67).*

In regard to claim 60, Jibbe teaches an analyzer as recited in claim 55 wherein the analyzer has at least one data capture mode selected from the group consisting of state mode (*status, fig. 5, 535)*, transitional timing mode (*statistic/time stamp, fig. 5, 540)*, and fixed frequency mode (*data payload, fig. 5, 530, col. 14 lines 27-29).*

In regard to claim 61, Jibbe teaches an analyzer as recited in claim 55 further comprising trigger logic that asserts a trigger signal when data presented to it matches a predefined pattern or sequence (*specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4).*

In regard to claim 62, Jibber teaches an analyzer as recited in claim 55 further comprising stop logic (*stop button is used to cause the analyzer to stop manipulating data, fig. 2, 245, col. 7 lines 66-67).*

In regard to claim 63, Jibbe teaches an analyzer as recited in claim 55 further comprising trigger logic (*specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4).*

In regard to claim 65, Jibbe teaches an analyzer as recited in claim 55 further comprising an event statistics counter which generates statistical information based on replayed data (*Statistical information relating to performance is tabulated, col. 9, lines 39-43).*

In regard to claim 66, Jibbe teaches an analyzer as recited in claim 55 wherein said replay logic selects whether data presented to internal functions of the analyzer comes from said trace buffer or from said data input port (*host-side monitor capture data file provides input to system or reads the template data structure to performs a performance analysis, col. 9 lines 31-34 and col. 10 lines 36-39).*

In regard to claim 67, Jibbe teaches an analyzer as recited in claim 55 wherein said trace buffer control logic includes stop logic (*stop button is used to cause the analyzer to stop manipulating data, fig. 2, 245, col. 7 lines 66-67)*, an address controller (*C/D, add, fig. 4, 432)*, and a memory controller (*disk array controller, fig. 1, 115, 120).*

In regard to claim 68, Jibbe teaches an analyzer as recited in claim 55 wherein said trace buffer control logic latches an address value of replay data (*in command phase an address are*

used to set up a particular type of data transfer, col. 11 lines 45-55).

In regard to claim 69, Jibbe teaches an analyzer as recited in claim 68 wherein said address value is latched to a FIFO (*performance analysis involves scanning through captured data stored in queue, col. 9 lines 34-38).*

In regard to claim 70, Jibbe teaches an analyzer as recited in claim 55 wherein the analyzer is capable of replaying traffic using the same timing that it was captured with (*played back with a time button for set at 00:00:00 for the beginning of a file, fig. 2, 210, col. 7 lines 31-35).*

In regard to claim 71, Jibbe teaches an analyzer as recited in claim 55 wherein the analyzer can perform any decoding (*decoder, fig. 4, 410)*, flagging (*selection phase, fig. 4, 420)*, finding (*performance analysis, fig. 4, 470)*, sorting (*interpreter/organizer, fig. 4, 445*, statistics (*statistical information are tabulated, col. 9 lines 39-41)* and filtering operations (*filters useless information from the set of template data structure, col. 12 lines 14-16)* of which it is capable using triggering and counting hardware that are also used for data capture purposes (*captured data file, fig. 4, 405).*

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14. Claims 72 and 75-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Blatter et al. (US 6,236,694).

In regard to claim 72, Jibbe teaches an analyzer for capturing activity on a transmission medium, comprising:

(a) a data input port for receiving the activity from the transmission medium (*point to point connection exist between a single host computer and a single disk array controller, fig. 1, 105, 115, col. 5 lines 5-12),*

(b) replay logic for receiving the activity from the data input port and receiving stored activity from a trace buffer and sending out one or the other of these activities to the trigger logic, but not both (*if state variable P/A is set to one the process next reads the template data structure generated and performs a performance analysis and if P/A is set to zero the process is next operative to play the template data structure file back on the reference system, fig. 3, 330, 325, col. 9 lines 31-46),*

(c) a trace buffer for receiving activity from said replay logic and storing it (*set of template data structures is stored in a data file, col. 1-5),* and for sending stored activity to said replay logic (*template data structure may be played out to emulate the behavior of a host computer, col. 9 lines 46-49)* and to a data output port (*generates an output which includes a set of template data structure, fig. 3, 315, col. 9 lines 2-4),*

(d) trigger logic for comparing the pattern of activity from the replay logic with a user-defined pattern of activity and indicating when they match (*search through a captured data file for a specific event or to specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4),*

(e) trace buffer control logic for causing activity from said replay logic to be either read from or written to said trace buffer (*record button is to capture data as observed by host-side monitor and the play button is used to caused on a sequence of data packets capture to be reproduced in the reference system, col. 8 lines 5-35),*

(f) a data output port for transferring stored activity in the trace buffer elsewhere for processing or display (*output is preferably stored in a data file but stream I/O may be used, col. 9 lines 4-5)*, and

(g) a control port for controlling modes of operation of the analyzer and for accepting user-defined patterns for triggering (*monitor and analyzes data transfer generated in the references system may be practiced with affair amount of intervention from the technician using GUI window and the submenus, fig. 2, 200, col. 9 lines 53-64).*

Jibbe does not explicitly teach the trigger logic includes time counters for using the relative time of occurrence of an activity event as part of its activity pattern comparison.

Blatter et al. teach the bus and interface system implementing a compares of the replayed timestamp value with a continuously changing count value produced by counting a free running oscillator (*col. 9 lines 13-24).*

It would have been obvious to modify the analyzer of Jibbe by adding Blatter et al. bus and interface system. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would facilitate the elimination of data timing perturbations and discontinuities resulting

from record/replay processing and enable the recorded signal timing to be restored (*col. 1 lines 63-67).*

In regard to claim 75, Jibbe teach an analyzer as recited in claim 72 further comprising selective capture logic for causing the trace buffer control logic to cause the activity from the replay logic to be written to the trace buffer (*record button is to capture data as observed by host-side monitor and the play button is used to caused on a sequence of data packets capture to be reproduced in the reference system, col. 8 lines 5-35)* only when the activity from said replay logic matches a second user-defined pattern of activity (*search through a captured data file for a specific event or to specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4).*

In regard to claim 76, Jibbe teach an analyzer as recited in claim 75 wherein said selective capture logic is capable of causing information about the type of activity from the replay logic that caused the activity to be written to said trace buffer to be incorporated into the activity stored in the trace buffer (*template data structure include a fourth field to stores input and output negotiation information respectively in a subfield, fig. 5, 520-522, col. 14 lines 12-24).*

In regard to claim 77, Jibbe teach an analyzer as recited in claim 75 further comprising a timestamp counter for creating information about the time of occurrence of each activity event from the replay logic, so that such information may be incorporated into the activity stored in

said trace buffer (*eight field of the template data structure stores the statistical information such as time-stamp associated with a data transfer, fig. 5, 540, col. 14 lines 31-33).*

In regard to claim 78, Jibbe teach an analyzer as recited in claim 77 wherein said trigger logic includes time counters for incorporating the relative time of occurrence of an activity event as part of its activity pattern comparison, and wherein said replay logic uses said stored time-of-occurrence information to control the timing of the replay (*a time button is used to enter or read a time representative of the beginning of a file or a specific event within a file in the system analyzer, fig. 2, 210, col. 7 lines 21-41).*

In regard to claim 79, Jibbe teach an analyzer as recited in claim 77 wherein said replay logic uses the stored time-of-occurrence information to control the timing of the replay (*a time button is used to enter or read a time representative of the beginning of a file or a specific event within a file in the system analyzer, fig. 2, 210, col. 7 lines 21-41).*

In regard to claim 80, Jibbe teach an analyzer as recited in claim 79 further comprising a replay output port for sending the activity from the replay logic to a transmission medium (*a view button caused certain types of information relating to data transfer activity to be displayed, fig. 2, 225, col. 7 lines 45-53).*

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15. Claims 73-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Blatter et al. (US 6,236,694) in further view of Nelson et al. (US 6,928,108).

In regard to claim 73, Jibbe and Blatter et al. does not teach an analyzer as recited in claim 72 wherein said trace buffer control logic includes logic for overwriting previously stored activity with new activity.

Nelson et al. teach the modem with firmware upgrade feature implementing a protect switch when not enable would not prevent overwriting of the program area of the flash prom (*col. 13 lines 1-7).*

It would have been obvious to modify the analyzer of Jibbe and Blatter et al. by adding Nelson et al. protect switch. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would provide a back door to allow access to the area of the flash PROM where the boot control program is stored (*col. 13 lines 1-7).*

In regard to claim 74, Jibbe and Blatter et al. does not teach an analyzer as recited in claim 72 wherein said trace buffer control logic includes logic for avoiding overwriting previously stored activity with new activity.

Nelson et al. teach the modem with firmware upgrade feature implementing a protect switch when not enable would not prevent overwriting of the program area of the flash prom (*col. 13 lines 1-7).*

Refer to claim 73 for motivational statement.

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16. Claims 81, 84-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Blatter et al. (US 6,236,694) in further view of Noy (US 7,114,111).

In regard to claim 81, Jibbe and Blatter et al. does not teach an analyzer as recited in claim 72 wherein activity events are stored at a fixed frequency, thereby providing a fixed time between events.

Noy teaches the method of maximizing test coverage by implementing the collection of data related to temporal coverage such as triggering event is optionally a fixed, predefined sampling time (*col. 8 lines 38-52).*

It would have been obvious to modify the method Jibbe and Blatter by adding Noy method of maximizing test coverage. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would allow temporal coverage (*col. 8 lines 40-46).*

In regard to claim 84, Jibbe and Blatter et al. does not teach an analyzer as recited in claim 72 wherein said replay logic uses the fixed time between events to send the stored activity out with the same timing with which it was received at the data input port.

Noy teaches the method of maximizing test coverage by implementing the collection of data related to temporal coverage such as triggering event is optionally a fixed, predefined sampling time (*col. 8 lines 38-52).*

Refer to claim 81 for motivational statement.

In regard to claim 85, Jibbe teach an analyzer as recited in claim 84 further comprising a replay output port for sending the activity from the replay logic to a transmission medium (*play the template data structure file back on the reference system, fig. 3, 330, 325, col. 9 lines 31-46).*

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17. Claim 82 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Blatter et al. (US 6,236,694) in further view of Lee et al. (US 6,377,643).

In regard to claim 82, Jibbe teach an analyzer as recited in claim 72 wherein said trigger logic is able to recognize for comparison purposes, patterns of activity that consist of a single event (*search through a captured data file for a specific event or to specify a trigger event which when detected will cause the recorder to start or stop capturing data, col. 8 lines 1-4)*

Jibbe and Blatter et al. does not teach an analyzer comparing patterns of activity that consist of a sequence of events.

Lee et al. teach the method of comparing a pattern matching sync signal output from a sync pattern detector according to clocks of the parallel clock generator (*col. 3 lines 6-10).*

It would have been obvious to modify the method Jibbe and Blatter et al. by adding Lee et al. pattern matching. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would solve the problem of deviation of a window caused by erroneous detection of a sync signal and disagreement of the numbers of clocks by using a specified window (*col. 1 lines 56-60).*

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18. Claim 83 is rejected under 35 U.S.C 103(a) as being unpatentable over Jibbe (US 6,687,856) in further view of Blatter et al. (US 6,236,694) in further view of Bucher et al. (US 2001/0016925).

In regard to claim 83; Jibbe and Blatter et al. does not teach an analyzer as recited in claim 72 wherein said trigger logic includes at least one counter for counting the number of occurrences of activity event as part of its activity pattern comparison.

Bucher et al. teach a deep trace memory system for a protocol analyzer implementing a read and a write counter (*paragraph 0030, fig. 4).*

It would have been obvious to modify the replay analyzer of Jibbe and Blatter et al. by adding Butcher et al. deep trace memory system for a protocol analyzer. A person of ordinary skill in the art at the time of applicant's invention would have been motivated

to make the modification because it would allow dual port memory to act as a fifo (*paragraph 0030).*

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Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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